23.7 A 300mW Programmable QAM Transceiver for VDSL Applications

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The VDSL Coalition specifies a QAM transceiver supporting higher data rates than ADSL [1]. VDSL provides a maximum data rate of 52Mb/s in downstream and 30Mb/s in upstream and features symmetric or asymmetric transmission to expand the area of applications. In this work, a complete physical layer (PHY) of a VDSL QAM transceiver including ADC, DAC, clock generator, and μ-controller interface is implemented using a 0.18μm CMOS technology. Measured power consumption is as low as 300mW, which is 1/3 of previous works [2]. Notable aspects of low power design and dual loop AGC architecture are presented.

Figure 23.7.1 shows a block diagram of the fabricated chip. The chip functionality can be divided into two layers: transmission convergence (TC) and physical medium dependent (PMD). The TC functions as an interface for certain transport protocols, and includes a framer. The PMD specifies the electrical characteristics of the transmit signal, coding, modulation, and duplexing methods.

At the TC layer, this transceiver supports several transport protocols such as UTOPIA level 1, 2, and a general-purposed serial/parallel interface. A scrambler uses a self-synchronous algorithm with generator polynomial, $x^{23}+x^{18}+1$. A RS codec is defined by a generator polynomial $g(x) = (x+\alpha^0)(x+\alpha^1)...(x+\alpha^{15})$ and primitive polynomial $p(x) = x^8+x^4+x^3+x^2+1$. A convolutional interleaver is included in order to improve the error correcting capability of the RS codec. 8kB internal memory is embedded for the UTOPIA and the interleaver.

At the transmit side of the PMD layer, a symbol-mapper converts the byte stream into 4-, 8-, 16-, 32-, 64-, 128-, and 256-QAM symbol stream. The pulse-shaping filter using a square root raised cosine with roll of factor (α=0.2) reduces the out-of-band power. Fixed-rate and linear interpolation algorithms are used to match the symbol to sampling rate. The fixed rate interpolator increases the data rate by one, two or four and the linear interpolator generates the data at the sample rate. The DA compensation filter was implemented to reduce the distortion effect of the sample-and-hold function in the DAC. The 12b DAC based on a segmented current source architecture operates at 100MS/s rate. Its SFDR was measured as 64dB at 75MS/s and 58dB at 100MS/s.

The frequency range from 1 to 10MHz in the VDSL spectrum is shared by amateur radio. It is well known that the amateur radio receiver is very sensitive to interference and the band definition is different for different countries. Therefore, the VDSL transmitter should be designed not only to reduce its signal power in the amateur radio bands but also to be programmable. For this purpose, the transmitter implements a notch filter with 2nd order IIR structure, as shown in Fig. 23.7.2, lowering the signal power by 20dB. The notches can be placed at any frequency of the band by programming the coefficients. Three IIR notch filters are integrated so that up to three notch points can be programmed. Figure 23.7.3 shows the spectrum of the transmit signal with three notches at 1.8MHz, 3.5MHz, and 7MHz. It was measured at 6.48MHz symbol rate and 5.39MHz center frequency and the attenuation was about 25dB.

At the receive side of the PMD layer, the ADC has 11b resolution, 70MS/s sampling rate, and a differential pipeline structure. The decimator is designed with a simple linear interpolation algorithm, and followed by a decision feedback equalizer (DFE) implemented with a signed LMS algorithm. The error functions for the timing recovery and the carrier recovery are given by

$$e_n = \mathrm{Re}\left\{r_n^* \times \left(r_{n+1/2} - r_{n-1/2}\right)\right\} \quad (1)$$

$$e_n = \mathrm{Im}\left\{d_n^* \times y_n\right\} \quad (2)$$

where r_n, d_n, and y_n stand for the received signal, the decision, and the equalized signal at nth symbol clock respectively.

In order for the receiver to achieve the maximum SNR, the received signal must be amplified to the full input range of the ADC. When the signal is amplified too much, it will be distorted by saturation causing SNR degradation. Conventional AGC's have been implemented based on the first-order tracking loop with a reference value, P_{REF} without any consideration about saturation [3]. However, it has been found out through extensive simulations that P_{REF} should be varied according to the center frequency, the symbol rate, and the channel length. Therefore, an AGC should also adjust P_{REF} automatically to maximize the BER performance.

The proposed dual loop AGC shown in Fig. 23.7.4 has an auxiliary loop for controlling P_{REF} in addition to a conventional gain control loop. The auxiliary loop receives the saturation bit of ADC. If the saturation occurs, P_{REF} is decreased by the step size Δ_{DOWN}. Otherwise, P_{REF} is increased by the step size Δ_{UP}. Throughout these operations, the auxiliary loop of AGC keeps the ADC output from saturating and sets the ADC input to its full range. The gain control loop of AGC must have wider bandwidth than the auxiliary loop to keep the AGC stable. Since the objective of the auxiliary loop is to avoid saturation of the ADC, Δ_{DOWN} is set to a larger value than Δ_{UP}.

Several techniques are used to reduce both the power consumption and silicon area. Filters with fixed coefficients were made with the multiplierless filter structure of canonic sign digit (CSD) description. Smaller size buffers for the taps of a DFE, a RS decoder, etc. are implemented with faster and smaller register files instead of using D flip-flops and a SRAM memory. A DFE adopting a resource-sharing algorithm was implemented with fully pipelined structure. Using only two LMS engines and two filter taps, an adaptive DFE supporting up to 32 feed-forward and 32 feedback taps was implemented. An internal clock source generates the clocks of each sub-block separately, and thereby further reduction of power is possible by independent control of the clocks to the unused blocks.

Figure 23.7.5 shows the recovered constellations of 16-QAM at 3000ft and 4-QAM at 9000ft with a BER<10^{-7}, exceeding the specification. These data are read from the internal control registers through μ-controller interface. The IC consumes less than 300mW at 30Mbps symmetric transmission, including I/O buffers. This chip was fabricated in a 0.18μm 1P6M CMOS process and the chip size is 5mm x 5mm. Figure 23.7.6 is the chip micrograph and Fig. 23.7.7 summarizes the chip specifications.

References

[1] "Very-high-speed Digital Subscriber Lines (VDSL): Transceiver Draft Technical Specification," VDSL Coalition, March 2000.
[2] R. B. Joshi, et al., "A 52Mb/s Universal DSL Transceiver IC," *ISSCC Digest of Technical Papers*, pp. 250-251, Feb. 1999.
[3] L. J. D'Luna, et al., "A Single-Chip Universal Cable Set-Top Box/Modem Transceiver," *IEEE J. Solid State Circuits*, vol. 34, No. 11, pp. 1647-1660, Nov. 1999.

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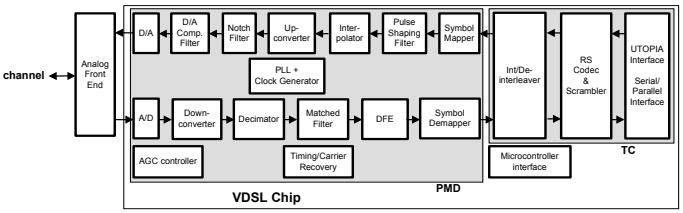
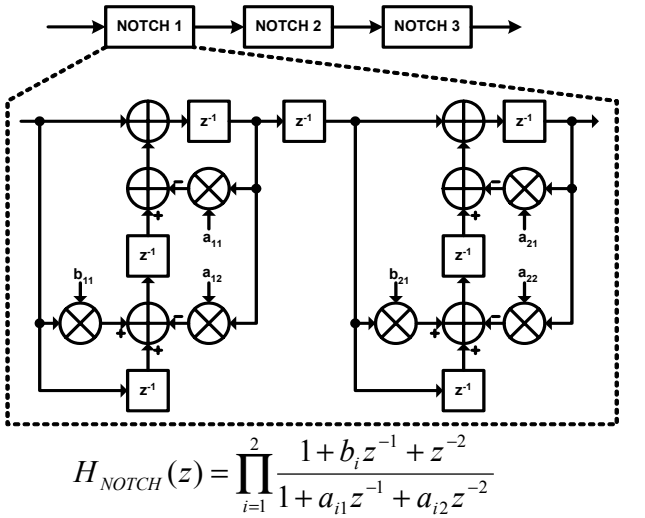


Figure 23.7.1: Block diagram of the VDSL transceiver.



$$H_{NOTCH}(z) = \prod_{i=1}^{2} \frac{1 + b_i z^{-1} + z^{-2}}{1 + a_{i1} z^{-1} + a_{i2} z^{-2}}$$

Figure 23.7.2: IIR notch filter.

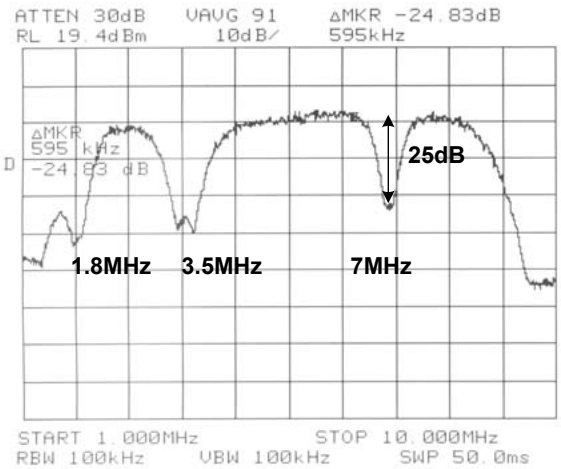


Figure 23.7.3: Measured spectrum of transmitted signal with three notches.

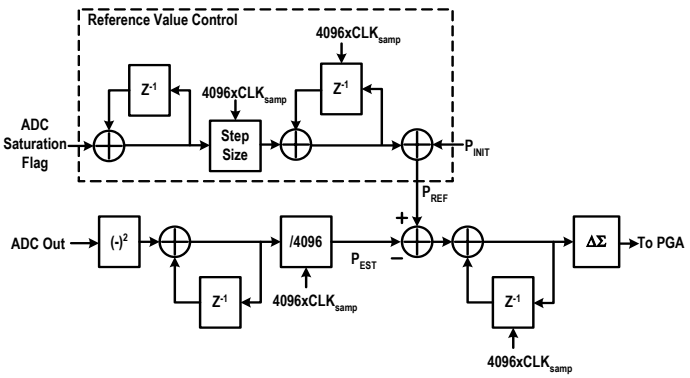


Figure 23.7.4: Block diagram of the dual loop AGC.

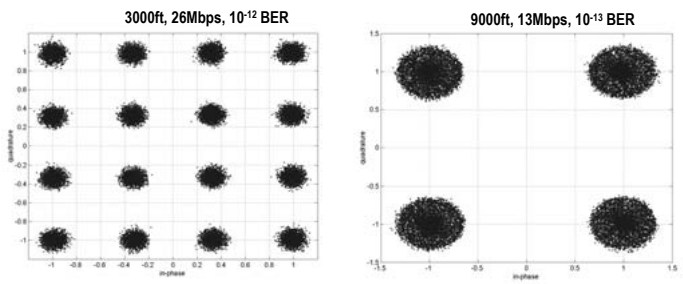


Figure 23.7.5: Measured constellation at 6.48MHz symbol rate.

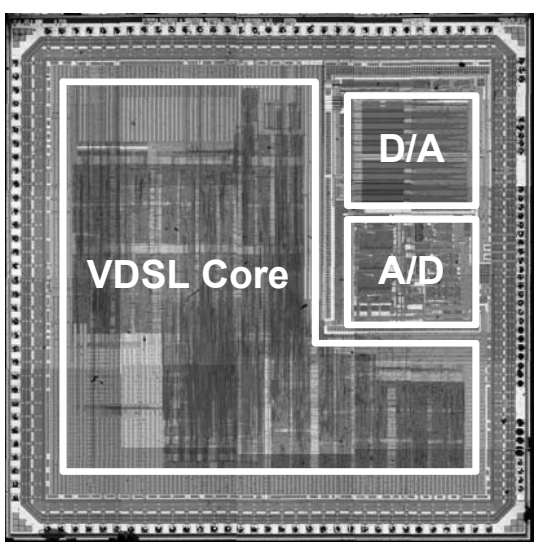


Figure 23.7.6: Chip micrograph.

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Technology	0.18μm 1P6M CMOS
QAM modes	4, 8, 16, 32, 64, 128, and 256
A/D converter	11bit, 70Msps
D/A converter	12bit, 100Msps
Package	100pin PQFP
Power Supply	1.8V (core) and 3.3V (I/O)
Power consumption	300mW @ 30Mbps symmetric
Data rate	13Mbps at 9000ft channel
Chip size	5mm x 5mm

Figure 23.7.7: Chip specification.

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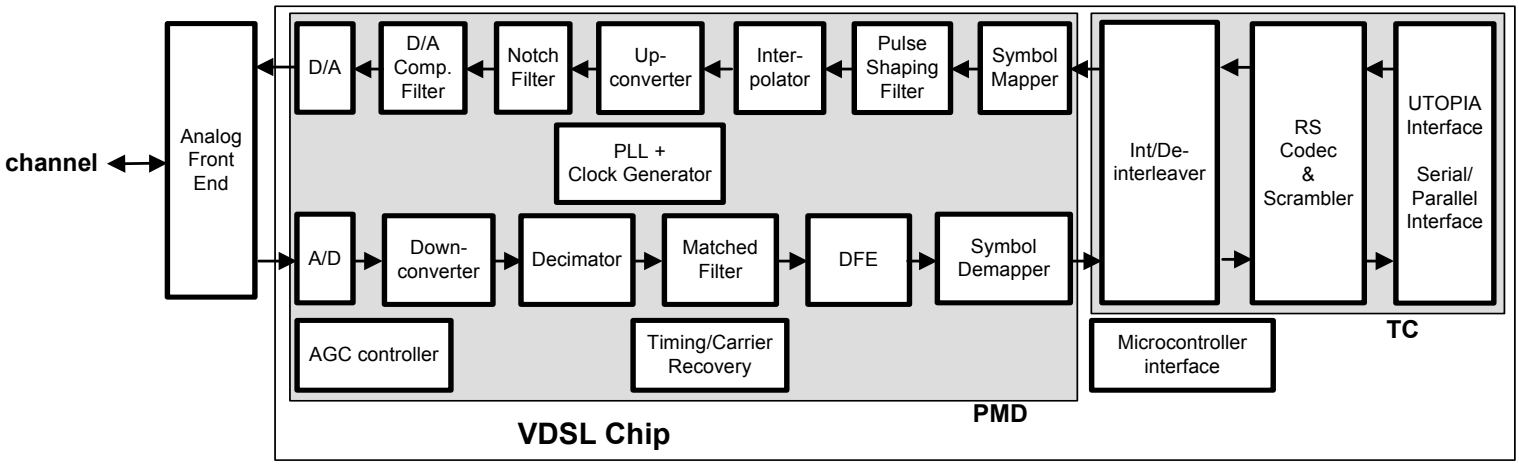

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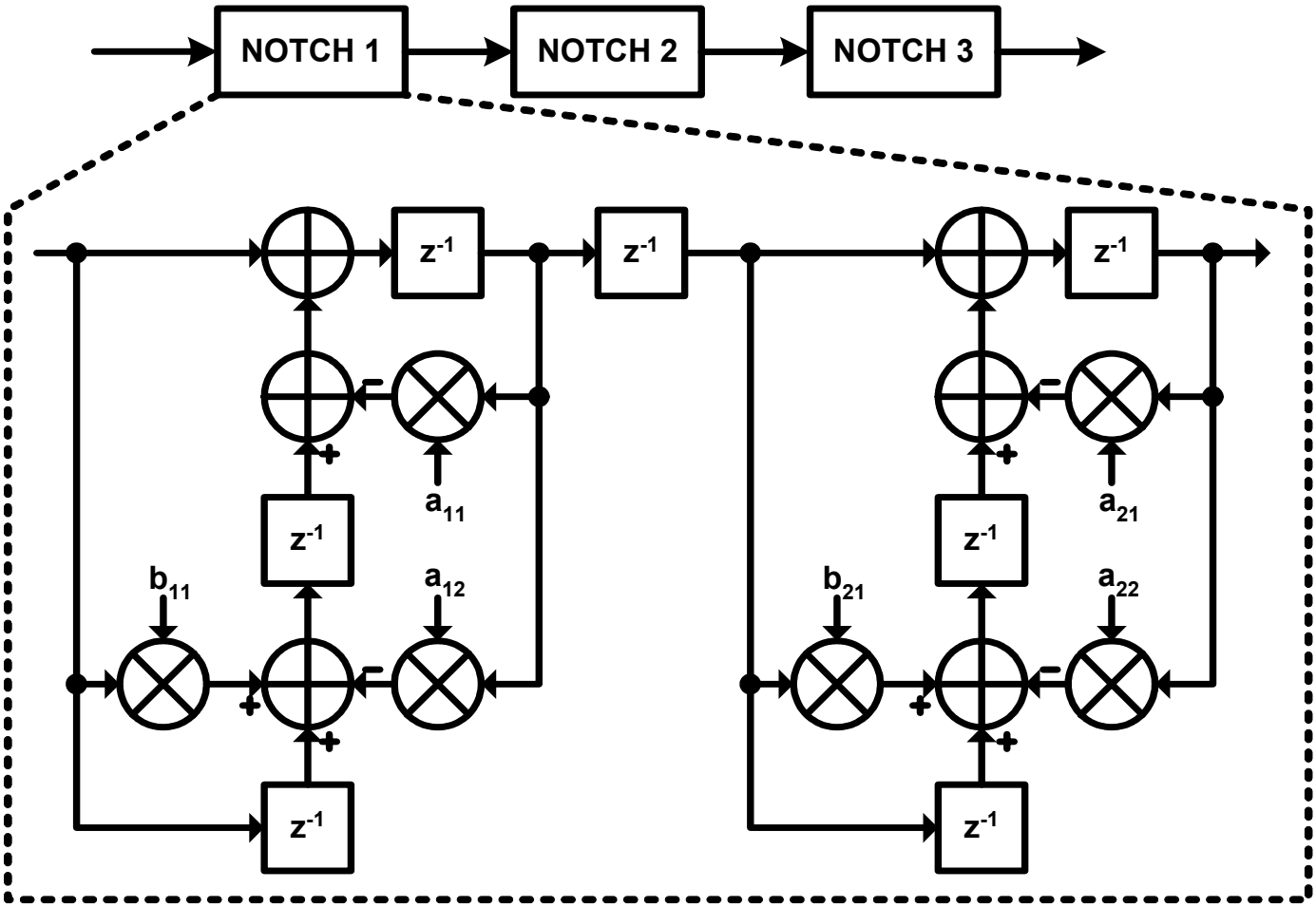

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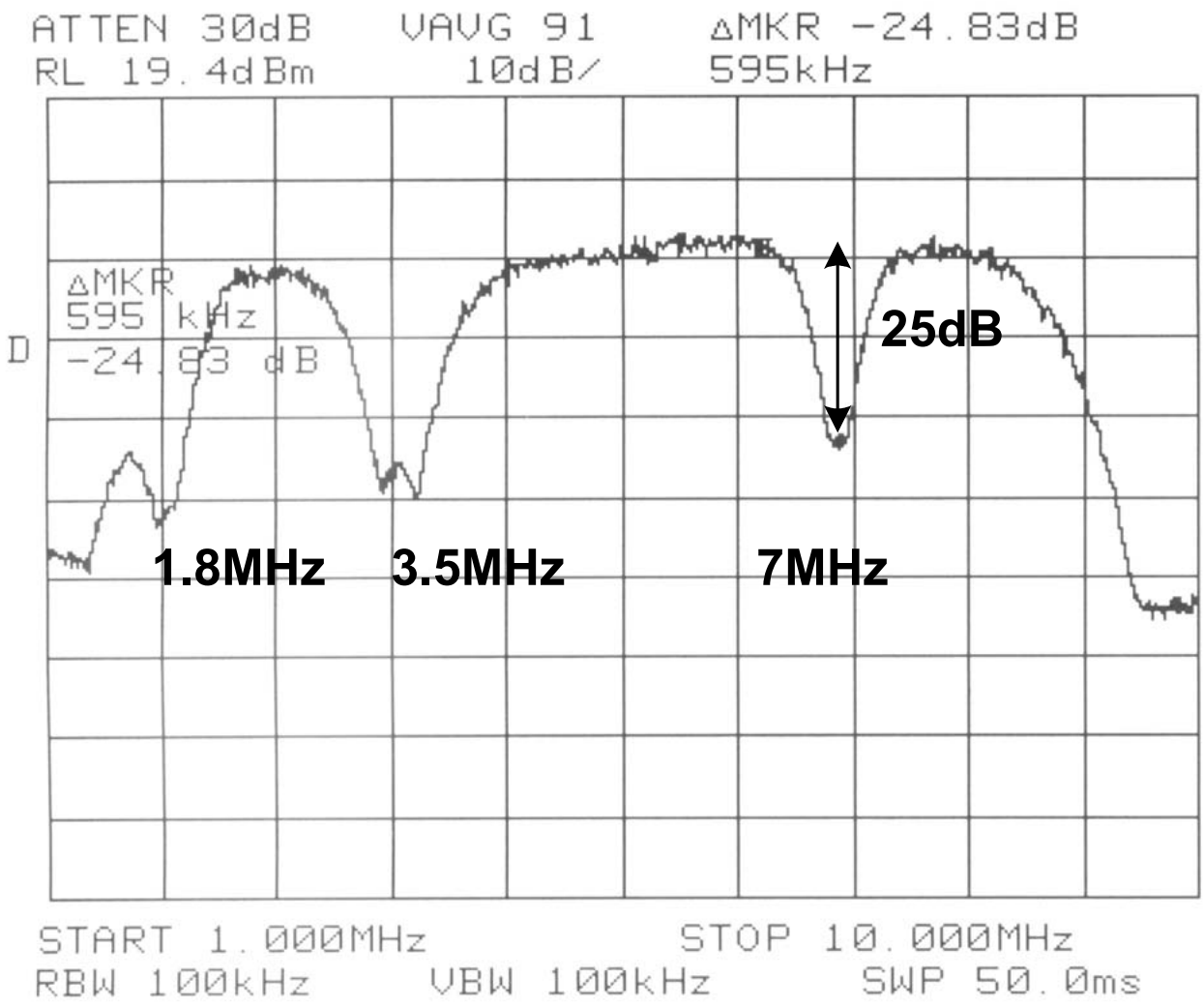

Figure 23.7.3: Measured spectrum of transmitted signal with three notches.

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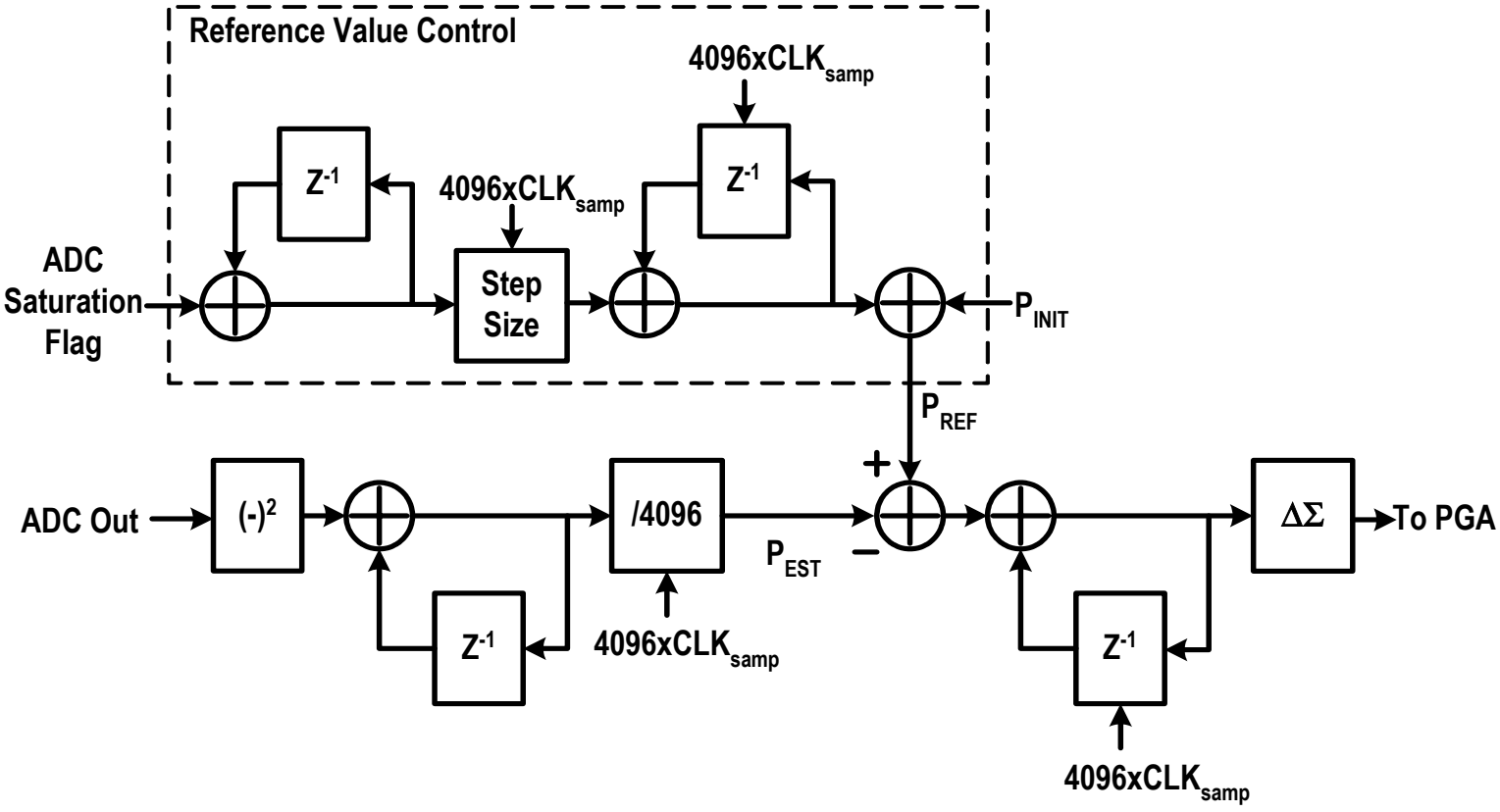

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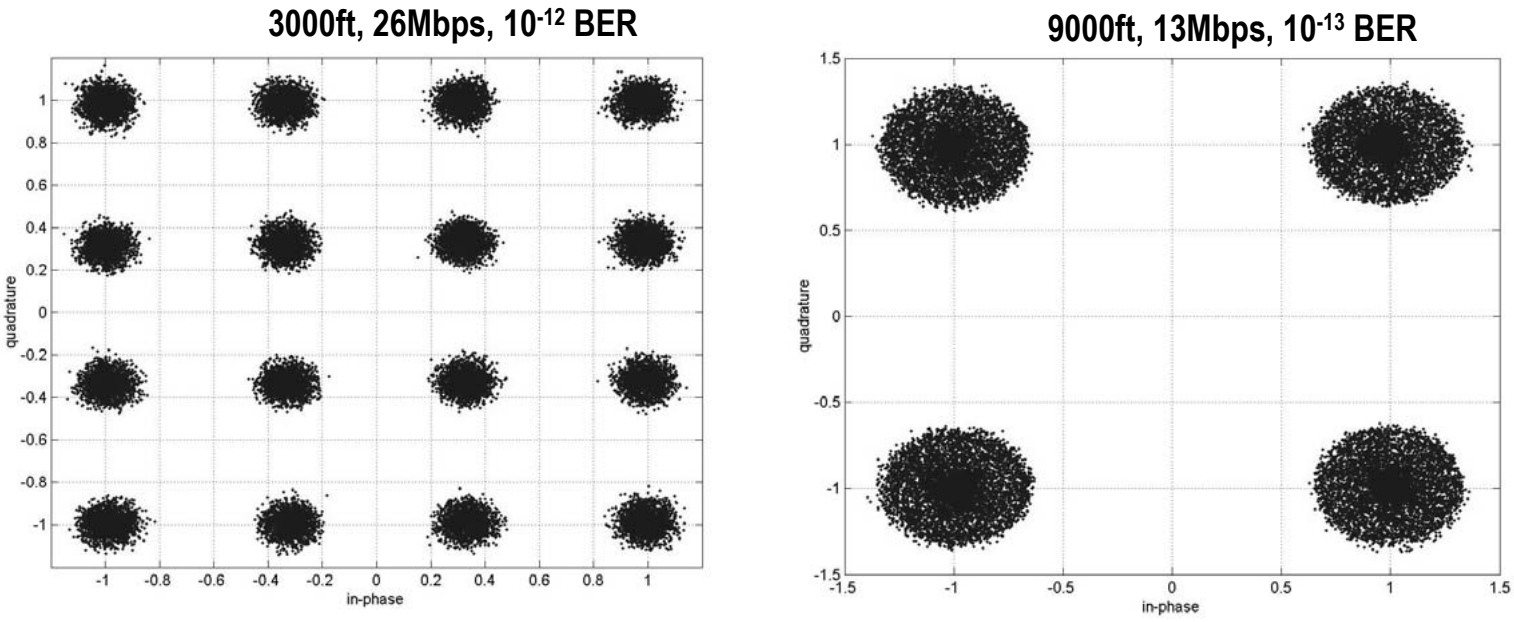

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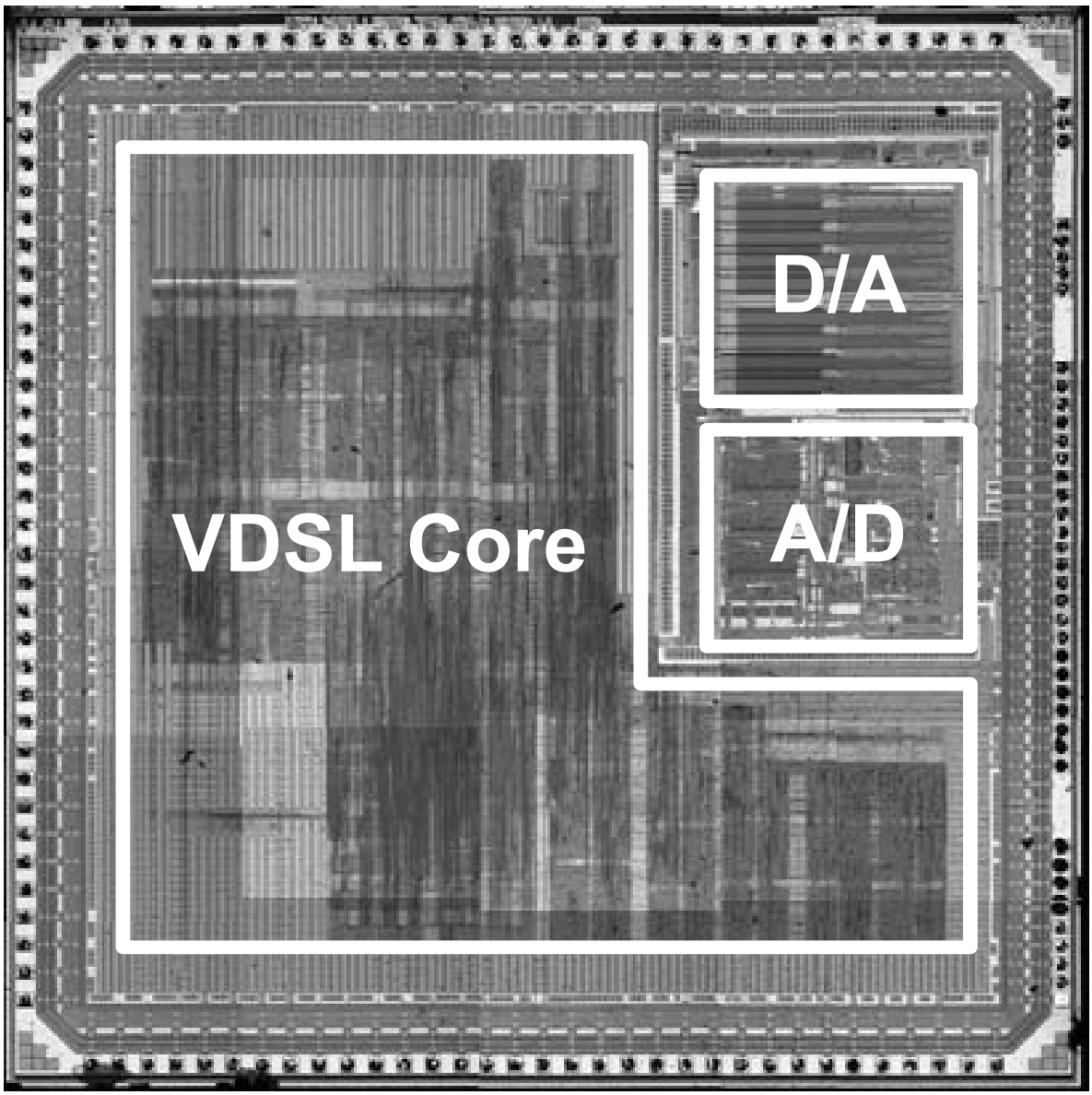

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